ABSTRACT:

A digital microelectronic circuit comprises a clocked data-processing unit (1) and a converting unit (2) which reads in data present at the output of the data-processing unit, performs a predetermined converting operation on the data and passes on the converted data. The converting unit is realized in an asynchronous logic circuit, such that the period of time for performing the converting operation is shorter than the shortest time interval to the next change of the data present at the output of the data-processing unit. In this way, fast, serial synchronous processes can be parallelized from the point of view of the slow synchronous system in synchronous systems which are slow relative thereto by using asynchronous logics, without a further high-frequency clock system being required.